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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 09/820,735  | 03/30/2001  | Yojiro Matsueda      | 109098              | 4744             |
| 25944   | 7590        | 06/10/2004           | EXAMINER            |                  |
| OLIFF & BERRIDGE, PLC<br>P.O. BOX 19928<br>ALEXANDRIA, VA 22320 |             |                      | KOVALICK, VINCENT E |                  |
|   |             |                      | ART UNIT            | PAPER NUMBER     |
|   |             |                      | 2673                |                  |
| DATE MAILED: 06/10/2004   |             |                      |                     |                  |

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                        |                     |  |
|------------------------------|------------------------|---------------------|--|
| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |  |
|                              | 09/820,735             | MATSUEDA, YOJIRO    |  |
|                              | <b>Examiner</b>        | <b>Art Unit</b>     |  |
|                              | Vincent E Kovalick     | 2673                |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 07 April 2004.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,2,4-16,18,19,21-30,32 and 34-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) 28 and 29 is/are allowed.
- 6) Claim(s) 1,2,4,6,9,13-16,19,22-25,32 and 34-38 is/are rejected.
- 7) Claim(s) 5,7,8,10-12,18,21,26,27 and 30 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

|  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input checked="" type="checkbox"/> Interview Summary (PTO-413)          |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date. _____ .  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>28-11/12/03</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____ .                                  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is in response to Applicant's Amendment dated April 7, 2004 in response to USPTO Office Action dated January 15, 2004. The amendments to claims 1-2, 4-8, 14, 16, 18-19, 21-29 and 34; the cancellation of claims 3, 17, 20, 31 and 33; the addition of new claims 36-38 and applicant's remarks have been considered and entered in the record.

Applicant's arguments filed April 7, 2004 have been fully considered but they are not persuasive. Regarding Applicant's argument relative to independent claims 1, 2, 14 and 34 and their relative dependent claims indicating that the prior art Okumura et al. (USP 5,945,972) does not teach a display device wherein "each of the static circuits storing a data signal supplied from a respective different one of the plurality of data lines". Okumura et al. teaches a pixel control circuit wherein data from the signal lines (Fig. 3, lines Lbj and Lcj) feed the memory units of the control circuit; in addition the memory units can also receive signals from the 'rewrite director' (Fig. 3, item 124) through the Sr input lines, in this manner each of the memory units can receive input signals from different input lines. It should be noted that with the variety of ways that data can be input to the memory units, and the argument as to the merits of the different implementations of these various input means, applicant would have to substantiate what is novel in using individual signal lines to feed data to each of the memory units.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2, 32 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (USP 5,945,972).

Relative to claims 1 and 2, Okumura et al. **teaches** a display device that has memory circuits each of which stores an image signal for a respective one of the pixels and that controls the writing of image signals into the pixels from the memory circuits in accordance with control signals (col. 2, lines 23-65 and col. 3, lines 1-11); Okumura et al. further **teaches** a display device, comprising: a plurality of write lines; a plurality of data lines; a plurality of dots disposed correspondingly to intersections between the plurality of write lines and the plurality of data lines, each of the plurality of dots for displaying including (col. 17, lines 23-31 and Fig. 6): a storing section having a memory cell configured by a static circuit, each of the static circuits storing a data signal supplied from a respective different one of the plurality of data lines (col. 14, lines 7-25);

wherein said storing section having a first static circuit and a second static, the first static circuit storing a first data signal supplied through a first data line of the plurality of data lines, and the second static circuit storing said second data signal supplied through a second data line of the plurality of data lines; and a display control section that performs display control on the basis of

Art Unit: 2673

the data signal held by the storing section (col. 17, lines 23-35 and Figs. 3 and 9); wherein said display control section performs tonal control on the basis of the data signal including the first data signal and the second data signal held by the storing section.

The difference between the teaching of claim 1 of the instant invention and that of Okumura et al. is that Okumura et al. does not specifically teach each of the static circuits storing a data signal supplied from a respective different one of the plurality of data lines directly driving the static circuits; whereas Okumura et al. accomplishes the same end result by utilizing a signal path either driving the storage units directly under control of storage unit selection means or using an alternate data signal path through "rewrite director" (Fig. 3, item 124) means.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Okumura et al. the feature of including the storing section in the memory cell in order to make the said storing section more compact in that it would contain both the memory elements and the display elements in the same unit as opposed to having the means (logic and signal channels) to transport the tonal level data from a storage source not co-resident with the display element.

Relative to claim 32, Okumura et al. further **teach** said display device wherein each of the plurality of dots further comprises an electro-optical conversion section that performs an electro-optical conversion on the basis of a data (col. 17, lines 23-55 and col. 18, lines 27-41 and Fig. 9).

Regarding claim 36, Okumura et al further **teaches** said display device wherein a number of the memory cells corresponds to a tonal level, a degree of the tonal level being determined by the data signal stored by the memory cells (col. 14, lines 7-19 and Abstract).

Art Unit: 2673

4. Claims 13 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. as applied to claim 2 in item 3 hereinabove, and further in view of Uragami et al. (USP 5,515,068).

Relative to claim 13 Okumura et al. **does not teach** a display control section controlling light emission of current-driven luminescent devices in connection on the basis of the analog signal in place of performing tonal control using a liquid crystal thereby effecting tonal control.

Okumura et al. teaches a display device including a substrate, a plurality of pixels arranged in rows and columns on the substrate and a plurality of signal lines for providing an image signal to the pixels on a column by column basis wherein each of the pixels comprises a plurality of memory elements for storing image signal sent over a corresponding one of the signal lines.

Uragami et al. **teaches** a semiconductor integrated circuit device to be utilized in a color palette device generating color pixel signals for a color display (col. 1, lines 64-67i and col. 2, lines 1-48); Uragami et al. further **teaches** said display device wherein the control section controlling light emission of current-driven luminescent devices in connection on the basis of the analog signal in place of performing tonal control using a liquid crystal, thereby effecting tonal control (col. 3, lines 44-67; col. 4, lines 1-5; col. 5, and col. 6, lines 32-37).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Okumura et al. the feature as taught by Uragami et al. in order to enable the system to drive an analog display device.

Regarding claim 37, Okumura et al. **does not teach** a display comprising a converting section that converts a value based on a value of the data signal held by the storing section into an analog value.

Art Unit: 2673

Okumura et al. teaches a display device including a substrate, a plurality of pixels arranged in rows and columns on the substrate and a plurality of signal lines for providing an image signal to the pixels on a column by column basis wherein each of the pixels comprises a plurality of memory elements for storing image signal sent over a corresponding one of the signal lines.

Uragami et al. **teaches** a semiconductor integrated circuit device to be utilized in a color palette device generating color pixel signals for a color display (col. 1, lines 64-67i and col. 2, lines 1-48); Uragami et al. further **teaches** said display comprising a converting section that converts a value based on a value of the data signal held by the storing section into an analog value (col. 4, lines 4-10 and col. 6, lines 14-39).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Okumura et al. the feature as taught by Uragami et al. in order to enable the system to drive an analog display device

5. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. taken with Uragami et al. as applied to claim 37 in item 4 hereinabove, and further in view of Matsueda et al. (USP 6,384,806).

Relative to claims 4 and 6, Okumura et al. taken with Uragami et al. **does not teach** a display device an analog value being represented as a PWM waveform generated by the converting section; said converting section performing conversion into the analog signal at a constant period interval.

Okumura et al. taken with Uragami et al. teaches a display device including a substrate, a plurality of pixels arranged in rows and columns on the substrate and a plurality of signal lines for providing an image signal to the pixels on a column by column basis wherein each of the

pixels comprises a plurality of memory elements for storing image signal sent over a corresponding one of the signal lines with a converting section that converts digital signals to corresponding analog signals with a display control section that performs tonal control on the basis of the analog signal.

Matsueda et al. **teaches** a digital driver circuit for electro-optical device and electro-optical deice having the digital driver circuit (col. 2, lines 66-67; col. 3, lines 1-67; col. 4, lines 1-67; col. 5, lines 1-67; col. 6, lines 1-67 and col. 7, lines 1-48); Matsueda et al. further **teaches** a display device an analog value being represented as a PWM waveform generated by the converting section; with said converting section performing conversion into the analog signal at a constant period interval (col. 8, lines 60-65 and col. 9, lines 4-27 and Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the device of Okumura et al. taken with Uragami et al. with the DAC feature as taught by Matsueda et al in order to generate an input signal compatible with analog driven display devices.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. taken with Uragami et al. in view of Matsueda et al.; as applied to claim 6 in item 5 hereinabove and further in view of Osada et al. (USP 5,973,456).

Relative to claim 9, Okumura et al. taken with Uragami et al. in view of Matsueda et al. **does not teach** said display device wherein alternating current drive voltage corresponding to the constant period being applied to said display control section.

Okumura et al. taken with Uragami et al. in view of Matsueda et al. teaches a display device including a substrate, a plurality of pixels arranged in rows and columns on the substrate and a

Art Unit: 2673

plurality of signal lines for providing an image signal to the pixels on a column by column basis wherein each of the pixels comprises a plurality of memory elements for storing image signal sent over a corresponding one of the signal lines with a converting section that converts digital signals to corresponding analog signals with a display control section that performs tonal control on the basis of the analog signal.

Osada et al. **teaches** an electroluminescent display device having uniform display element column luminosity (col. 1, lines 61-67 and col. 2, lines 1-57); Osada et al. further **teaches** said display device wherein alternating current drive voltage corresponding to the constant period being applied to said display control section (col. 3, lines 12-22).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Okumura et al. taken with Uragami et al in view of Matsueda et al. with the feature as taught by Osada et al. in order to apply the alternating current to the display devices in a uniform time period.

7. Claims 14-16 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. as applied to claim 1 in item 3 hereinabove, and further in view of Kimura (USP 6,518,941).

Regarding claim 14, Okumura et al. **does not teach** said display device having a luminescent section including a plurality of luminescent elements having different areas; and an active devices section connected to the storing section and the luminescent section.

Okumura et al. teaches a display device including a substrate, a plurality of pixels arranged in rows and columns on the substrate and a plurality of write lines and data lines for providing image signals to the pixels on a column by column basis wherein each of the pixels comprises a

plurality of memory elements configured by a static circuit for storing image signal sent over a corresponding one of the data lines.

Kimura **teaches** a display device (col. 2, lines 19-67 and col. 3, lines 1-21); Kimura further **teaches** a luminescent section including a plurality of luminescent elements having different areas (col. 4, lines 7-11); and an active devices section connected to the storing section and the luminescent section (col. 2, lines 32-35; col. 3, lines 58-65 and Fig. 1).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the device of Okumura et al. with the features as taught by Kimura in order provide luminescent elements with the means to provide different luminous intensity levels , and with the means to turn the luminescent elements ON/OFF by means of the said active element (TFT).

Regarding claims 15-16, Kimura **teaches** the said display device wherein the plurality of luminescent elements are organic EL elements (col. 4, lines 7-11).

Regarding claim 38, Okumura et al further **teaches** said display device wherein a number of the memory cells corresponds to a tonal level, a degree of the tonal level being determined by the data signal stored by the memory cells (col. 14, lines 7-19 and Abstract).

8. Claims 19, 22-25 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. as applied to claim 1 in item 3 hereinabove, and further in view of Hebiguchi et al. (USP 6,583,777) taken with Smith (USP 6,278,428).

Regarding claims 19, 34 and 35, Okumura et al. further **teaches** the plurality of dots including an electro-optical section that performs an electro-optical conversion on the basis of the data signal held by the storing section (col. 17, lines 23-55).

Art Unit: 2673

Relative to claims 19 and 34-35 Okumura et al. **does not teach** a display device comprising an active-matrix section having a plurality of dots disposed correspondingly to intersections of the plurality of write lines and the plurality of data lines, or the write signal being supplied to only a dot to be written of the plurality of dots.

Okumura et al. teaches a display device including a substrate, a plurality of pixels arranged in rows and columns on the substrate and a plurality of write lines and data lines for providing image signals to the pixels on a column by column basis wherein each of the pixels comprises a plurality of memory elements configured by a static circuit for storing image signal sent over a corresponding one of the data lines.

Hebiguchi et al. **teaches** an active matrix type liquid crystal display device (col. 3, lines 5-67; col. 4, lines 1-67; col. 5, lines 1-67; col. 6, lines 1-67 and col. 7, lines 1-35); Hebiguchi et al. further **teaches** an active-matrix section having a plurality of dots disposed correspondingly to intersections of the plurality of write lines and the plurality of data lines (col. 8, lines 50-67; and col. 19, lines 52-62).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide the device of Okumura et al. with the active matrix control elements as taught by Hebiguchi et al. in order to provide a ON/OFF control means to each of the matrix display elements.

Okumura et al. in view of Hebiguchi et al. **does not teach** the write signal being supplied to only a dot to be written of the plurality of dots.

Okamura et al. in view of Hebiguchi et al. teaches an active matrix display device including a substrate, a plurality of pixels arranged in rows and columns on the substrate and a plurality of

write lines and data lines for providing image signals to the pixels on a column by column basis wherein each of the pixels comprises a plurality of memory elements configured by a static circuit for storing image signal sent over a corresponding one of the data lines. Smith discloses column and row decoders for a matrix display.

Smith **teaches** an active matrix liquid crystal display panel (col. 2, lines 52-67 and col. 3, lines 1-23); Smith further **teaches** the write signal being supplied to only a dot to be written of the plurality of dots (col. 3, lines 51-63; col. 5, lines 61-67; col. 6, lines 1-5 and Fig. 6).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Okumura et al in view of Hebiguchi et al. with the column and row decoder means in order to select the desired pixel to which a particular data signal is directed.

Regarding claim 22, Smith further **teaches** the said display device wherein the row decode section being allocated correspondingly to a length the active-matrix section in a column direction, and the column decoder section being allocated correspondingly to a length of the active-matrix section in a row direction. (Fig. 6).

Relative to claim 23, Smith further **teaches** the said display device further including a column selection switch section that transmits the data signal to a data line of the plurality of data lines selected by the column decoder section (col. 5, lines 6-20).

Regarding claims 24 and 25, Smith **teaches** the display device wherein the row decoder that selects a row of the plurality of write lines through which a write signal is transmitted on the basis of an address signal; and the column decoder section that selects a data line of the plurality of data lines on the basis of an address signal. It is well known and in common practice

in the art that the display element location to which a data signal is directed is originated from the address signal associated with the data.

***Allowable Subject Matter***

9. Claims 5, 7-8, 10-12, 18, 21, 26-27 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 5, the major difference between the teachings of the prior art of recored (USP 5,945,972, Okumura et al.), USP 5,515,068, Uragami et al., USP 6,518,941, Kimura ; USP 6,583,777, Hebiguchi et al. and USP 6,278,428, Smith) and that of the instant invention is that said prior art **does not teach** said display device wherein the analog value including gamma-characteristics.

Regarding claim 7, the major difference between the teachings of the said prior art of recored and that of the instant invention is that said prior art **does not teach** said display device wherein a duration that no conversion into the analog value is made being provided in the constant period.

Regarding claim 10, the major difference between the teachings of the said prior art of recored and that of the instant invention is that said prior art **does not teach** said display device wherein the alternating current drive voltage being a voltage driven at VCOM+/-Va with respect to a reference voltage VCOM.

Regarding claim 11, the major difference between the teachings of the said prior art of recored and that of the instant invention is that said prior art **does not teach** said display device wherein

Art Unit: 2673

the alternating current drive voltage being a voltage alternating-current-inversion-driven by two voltage-applying lines laid correspondingly to said dot array pattern.

Regarding claim 12, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device wherein a plurality of rows of said dot array being provided by groups, and rows in pair being set in each of the groups to invert a phase of the alternating current drive voltage applied.

Regarding claim 18, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device includes a plurality of read lines disposed correspondingly to the plurality of dots, read out of the data signal held by the storing section being performed when a read signal is transmitted through a respective different one of the plurality of read lines.

Regarding claim 21, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device comprising a plurality of first lines for supplying a voltage as a power source to the storing section, the plurality of first lines being shared between two rows of the plurality of write signal lines.

Regarding claim 26, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device including a plurality of pixels each of which being provided by three dots for red, green and blue, respectively, of the plurality of dots; the column decoder section selecting data lines of the plurality of data lines corresponding to a respective pixel of the plurality of pixels; and the data

signal being supplied together to the three dots included in a respective one of the plurality of pixels.

Regarding claim 27, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device including a plurality of pixels each of which being provided by three dots for red, green and blue, respectively, of the plurality of dots; the column decoder section selecting data lines of the plurality of data lines corresponding to respective pixels of the plurality of pixels; and the data signal being supplied together to the three dots included in the respective pixels.

Regarding claim 30, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device wherein the column selection switch section being allocated correspondingly to a length of the active-matrix section in a row direction.

10. Claims 28 and 29 are allowed.

11. The following is an examiner's statement of reasons for allowance:

Regarding claim 28, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device comprising a substrate wherein the plurality of write lines, the plurality of data lines, the active-matrix section, the column decoder section, the row decoder section and the timing controller section being integrally formed on the substrate.

Regarding claim 29, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art **does not teach** said display device comprising a substrate wherein the plurality of write lines, the plurality of data lines, the active-

Art Unit: 2673

matrix section, the column decoder section, the row decoder section and the memory controller section being integrally formed on the substrate.

*Conclusion*

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

|                  |           |                  |
|------------------|-----------|------------------|
| U. S. Patent No. | 6,388,661 | Richards         |
| U. S. Patent No. | 6,323,867 | Nookala et al.   |
| U. S. Patent No. | 6,258,606 | Kovacs           |
| U. S. Patent No. | 6,064,158 | Kishita et al.   |
| U. S. Patent No. | 5,841,897 | Nulmakura et al. |

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Responses***

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Vincent E. Kovalick  
June 4, 2004

  
BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600